UTO-NBL-51MA

Datasheet

2017

Version 01.4

Beyond the technology

Utovertek

VERSION HISTORY

REVISION	AMENDMENT	DATE	
01.1	Initial version		
01.2	Minor change		
01.3	Dimension Change		
01.4	Dimension Change		

DESCRIPTION

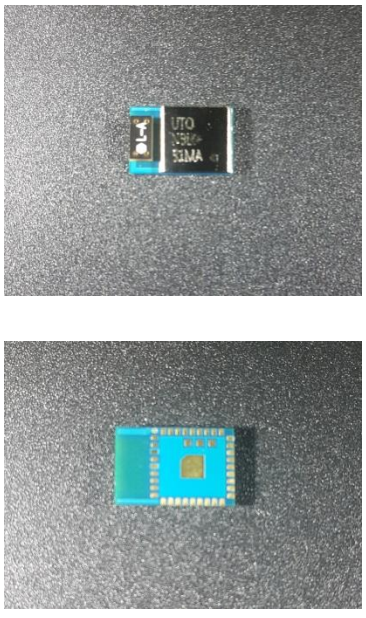
UTO-NBL-51MA is a built-in Antenna Bluetooth Low Energy Module. UTO-NBL-51MA integrates all features of Bluetooth radio, software stack, GATT based profiles, antenna and host end user applications, which means no external micro controller. It provides a Bluetooth Low Energy fully compliant system for a data communication. At +4 dBm TX Power and -93dBm RX Sensitivity UTO-NBL-51MA has best RF performance.

APPLICATION

- Commercial
- Sports and fitness
- Healthcare
- Medical sensors
- Home entertainment
- Mobile accessories
- Watch
- Human interface devices

FEATURE

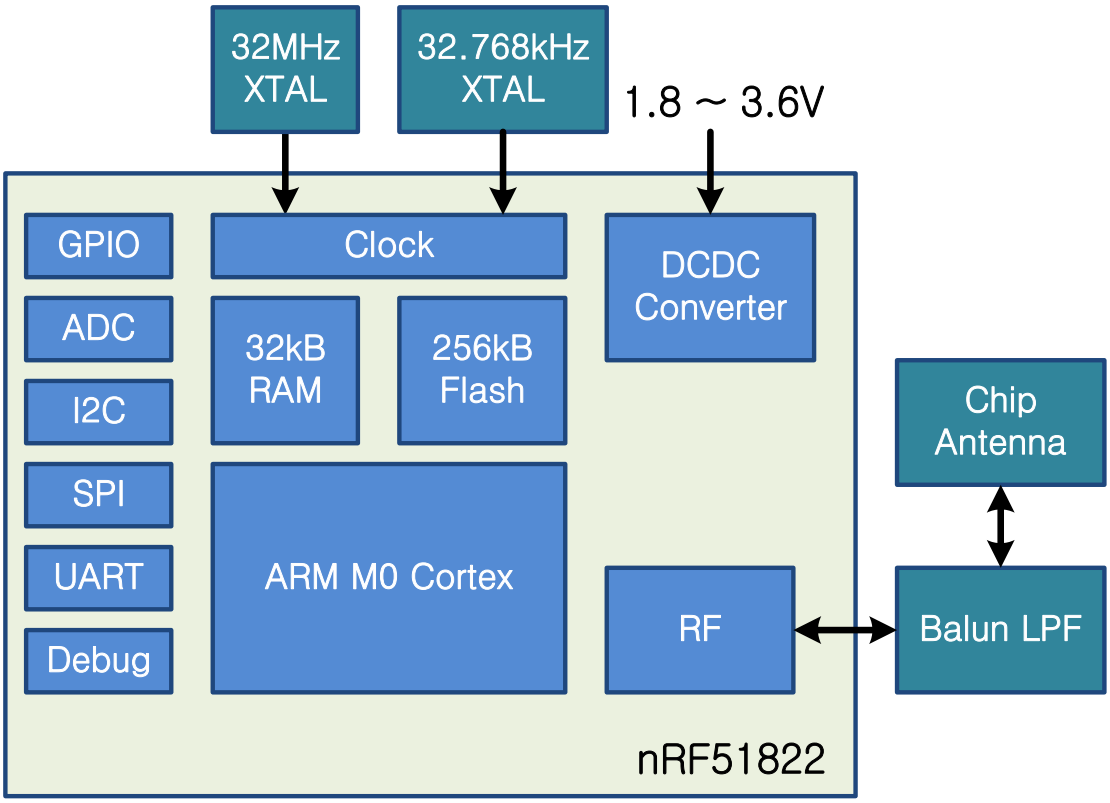
- Bluetooth v4.1 Single Mode Compliant
- Integrated Bluetooth Smart Stack
  . GAP, GATT, L2CAP and SMP
  . Bluetooth Smart profiles
- RF Performance
  . Transmit power : +4 dBm (-20 dBm ~ +4 dBm)
  . Receiver sensitivity : -93 dBm
- Low Power Consumption
  . Transmit : 10 mA peak (0 dBm)
  . Receiver : 13 mA peak
  . Sleep mode : 0.5 uA
- Peripheral Interfaces
  . UART/SPI(Master/Slave)/I2C
  . GPIO
  . 10-bit ADC
  . Timer
  . Temperature Sensor
- Power supply : 1.8 ~ 3.6 V
- Dimension : 6.4 x9.7 x 1.9 mm (W x L x H)



<Figure 1. UTO-NBL-51MA >

1. Block Diagram

UTO-NBL-51MA's block diagram is illustrated in Figure 2 below.



<Figure 2. Simplified block diagram of UTO-NBL-51MA>

CPU and Memory

The Main core is **ARM Cortex-M0**. By using a single-cycle 32 bit multiplier, a 3-stage pipeline, NVIC, the ARM Cortex-M0 CPU makes program execution simple and highly efficient.

The CPU use flash based memory in the code, FICR, and UICR regions. The embedded flash memory for program and static data can be programmed using SWD interface, or in-system from a program executing from code area. The Non-Volatile Memory Controller (NVMC) is used for program/erase operations. Regions of flash memory can be protected from read, write and erase by the Memory Protection Unit (MPU).

The **32-KB SRAM** of 1024 byte page size and **256-KB flash** of 8-KB block size memory are provided.

The **4-KB memory protection unit** can be configured to protect all flash memory on the device from read-back, or to protect blocks of flash over-write or erase.

Power management

UTO-NBL-51MA supports two different power supply alternatives of Internal LDO mode and Low voltage mode. In **internal LDO mode**, the system power is generated directly from the supply voltage VDD. In **low voltage mode**, the system power is supplied by 1.8V.

The module's power management features are System OFF mode and System ON mode. In **system OFF mode**, the module is in deepest power saving mode. The system's core functionality is powered down and all ongoing tasks are terminated.

In **system ON mode**, the module is fully operational and CPU and selected peripherals can be brought into a state where they are functional and more or less responsive depending on the sub-power mode selected by Low power or Constant latency.

Clock management

The module has a 32 MHz main crystal oscillator and 32.768 kHz RTC crystal oscillator.

Peripherals

The **general GPIO** is organized as one port with up to 30 I/Os enabling access and control of up to 30 pins through one port. Each GPIO can be accessed individually with the following user configurable features.

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system. The maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- All pins can be individually configured to carry serial interface or quadrature demodulator signals.

The **transceiver** receives and transmits data directly to and from system memory for flexible and efficient packet data management. The module's transceiver has the following features.

- General modulation features

  . GFSK modulation

  . Data whitening

  . On-air data rates (250 kbps/1 Mbps/2 Mbps)
- Transmitter with programmable output power of +4 dBm to -20 dBm, in 4 dB step
- RSSI function (1 dB resolution)
- Receiver with integrated channel filters achieving maximum sensitivity

(-96 dBm at 250 kbps/-93 dBm at 1 Mbps BLE/-90 dBm at 1 Mbps/-85 dBm at 2 Mbps)

- Baseband controller

  . EasyDMA RX and TX packet transfer directly to and from RAM

  . Dynamic payload length

  . On-the-fly packet assembly/disassembly and AES CCM payload encryption

  . 8 bit, 16 bit and 24 bit CRC check

The **Timer** will start requesting the 1 MHz mode of the HFCLK for values of the prescaler that gives F_timer less or equal to 1 MHz. If the timer module is the only one requesting the HFCLK, the system will automatically switch to using the 1 MHz mode resulting in a decrease in the current consumption. The task/event and interrupt features make it possible to use the PPI system for timing and counting tasks between any system peripheral including any GPIO of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any G{IO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The **Real Time Counter(RTC)** module provides a generic, low power timer on the low-frequency clock source(LFCLK). The RTC features a 24 bit COUNTER, 12 bit prescaler, capture/compare registers, and a tick event generator for low power, tickles RTOS implementation.

The **Random Number Generator(RNG)** generates true non-deterministic random number derived from thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

The **temperature sensor** measures die temperature over the temperature range of the device with 0.25 degree resolution.

The **SPI** interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data

transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The SPI peripheral supports SPI mode 0(Master), 1(Master), 2(Slave) and 3(Slave).

The **two-wire interface (TWI)** can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps and 400 kbps. The TWI peripheral supports TWI0 (Master), TWI1 (Master).

The **Universal Asynchronous Receiver/Transmitter (UART)** offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware up to 1 Mbps baud. Parity checking is supported.

The **quadrature decoder (QDEC)** provides buffered decoding of quadrature-encoded sensor signal. It is suitable for mechanical and optical sensors with an optional LED output signal and input debounce filters. The sample period and accumulation are configurable to match application requirements.

The 10 bit incremental **Analog to Digital Converter (ADC)** enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8, 9 and 10 bit)

A **GPIOTE** block enables GPIOs on Port 0 to generate events on pin state change which can be used to carry out tasks through the PPI system. Low power detection of pin state changes on Port 0 is possible when in System ON or System OFF. The number of GPIOTE channels is 4.

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the **low power comparator** can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Rating	Min	Max	Unit
Storage Temperature	-40	+125	Degree
VDD, VDD_RF	-0.3	3.9	V
Other Terminal Voltages	-0.3	VDD+0.3	V

<Table 1 : Absolutes Maximum Ratings>

2.2 Recommended Operating Conditions

Rating	Min	Max	Unit
Operating Temperature	-40	+105	Degree
VDD, VDD_RF*	1.8	3.6	V

<Table 2 : Recommended Operating conditions>

*) normal supply voltage is 3.0 ~ 3.3V

2.3 Current consumption

Power mode	Condition	Min	Typ	Max	Unit
Transmit	Pout = +4 dBm		16		mA
	Pout = 0 dBm		10.5		mA
Receive	At 250 kbps		12.6		mA
	At 2 Mbps		13.4		mA

<Table 3 : Current consumption>

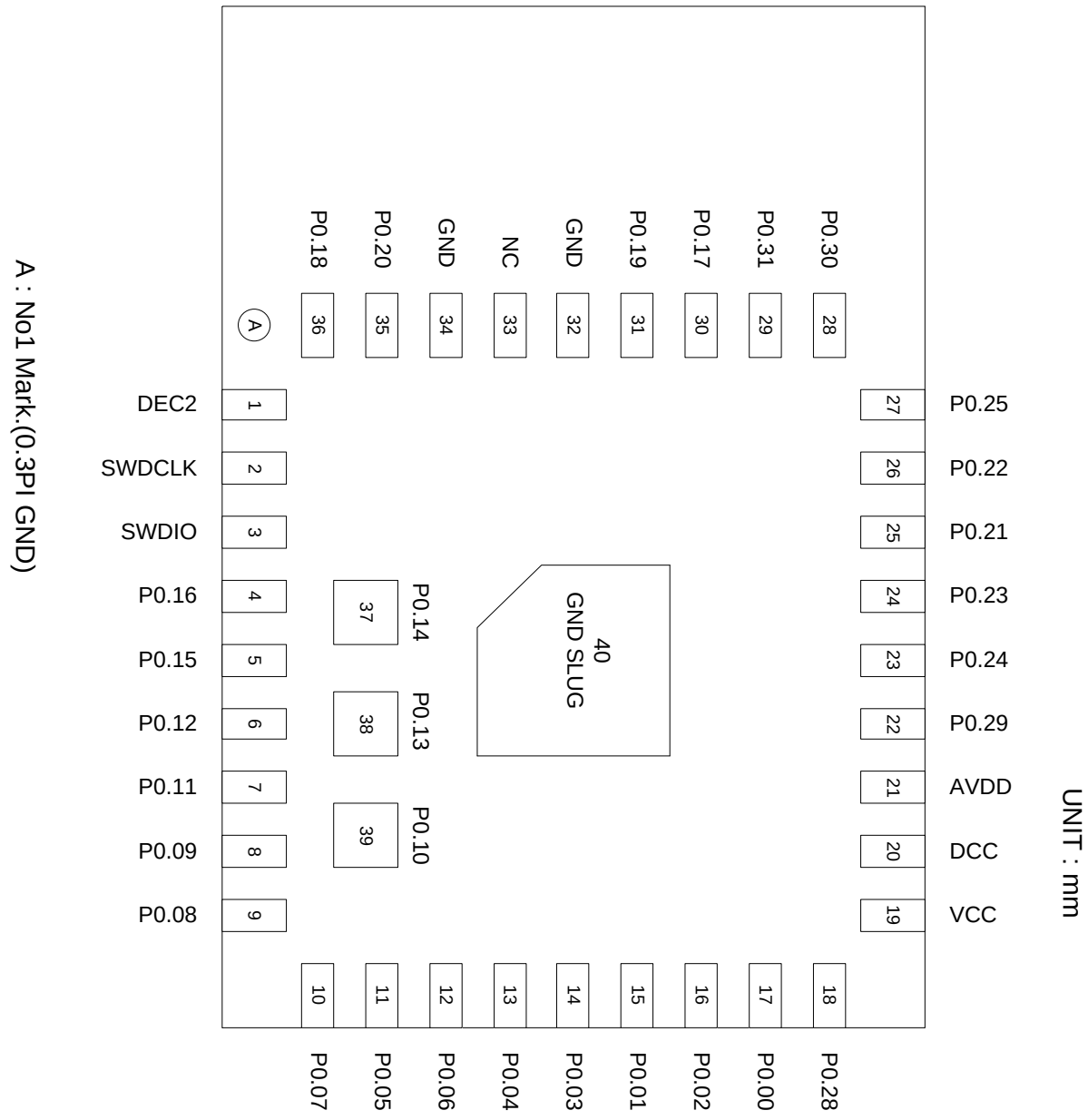
2.4 RF Characteristics

Rating	Min	Typ	Max	Unit
Operating frequencies	2400		2483	MHz
TX Maximum output power		4		dBm
TX RF power control range	20	24		dB
TX RF power accuracy			+/-4	dB
TX 20 dB bandwidth for modulated carrier		1800	2000	kHz
TX 1st Adjacent Channel Transmit Power (2 Mbps)			-20	dBc
TX 2nd Adjacent Channel Transmit Power (2 Mbps)			-45	dBc
TX 1st Adjacent Channel Transmit Power (1 Mbps)			-20	dBc
TX 2nd Adjacent Channel Transmit Power (1 Mbps)			-40	dBc
TX 1st Adjacent Channel Transmit Power (250 kbps)			-25	dBc
TX 2nd Adjacent Channel Transmit Power (250 kbps)			-40	dBc
RX maximum received signal strength at < 0.1% PER		0		dBm
RX Sensitivity (0.1% BER) at 2 Mbps		-85		dBm
RX Sensitivity (0.1% BER) at 1 Mbps		-90		dBm
RX Sensitivity (0.1% BER) at 250 kbps		-96		dBm
RX RSSI accuracy (-50 dBm to -80 dBm)			+/-6	dB
RX RSSI resolution		1		dB
RX RSSI sample period	8.8			us

<Table 4 : RF Characteristics>

3. Pin Description

UTO-NBL-51MA's PIN descriptions are summarized in Figure 3 and Table 5 below.



- Top View (Bottom pad)

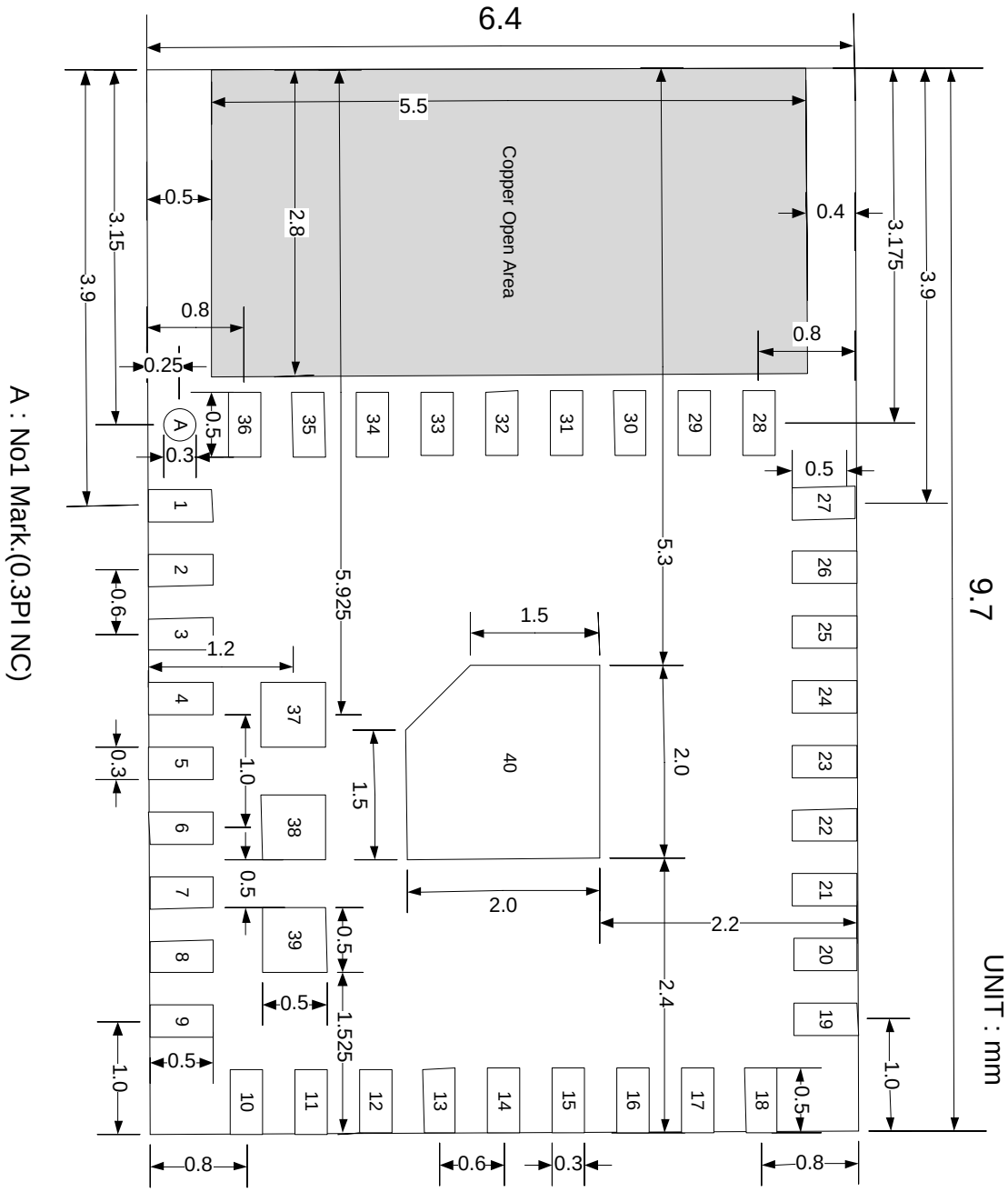
<Figure 3. PIN descriptions>

Num.	PIN Name	Type	Description
1	DEC2	Supply Voltage	1.8V supply in 1.8V mode (NC at 3.3V)
2	SWDCLK	DEBUG	Debug/Program
3	SWDIO	DEBUG	Debug/Program
4	P0.16	I/O	Configurable I/O
5	P0.15	I/O	Configurable I/O
6	P0.12	I/O	Configurable I/O
7	P0.11	I/O	Configurable I/O
8	P0.09	I/O	Configurable I/O
9	P0.08	I/O	Configurable I/O
10	P0.07	I/O	Configurable I/O
11	P0.05	I/O	Configurable I/O
12	P0.06	I/O	Configurable I/O
13	P0.04	I/O	Configurable I/O
14	P0.03	I/O	Configurable I/O
15	P0.01	I/O	Configurable I/O
16	P0.02	I/O	Configurable I/O
17	P0.00	I/O	Configurable I/O
18	P0.28	I/O	Configurable I/O
19	VCC	Supply Voltage	1.8V or 3.3V power supply
20	DCC	Power out	DC/DC output voltage to external LC filter
21	AVDD	Power in	Analog power supply(Radio)
22	P0.29	I/O	Configurable I/O
23	P0.24	I/O	Configurable I/O
24	P0.23	I/O	Configurable I/O
25	P0.21	I/O	Configurable I/O
26	P0.22	I/O	Configurable I/O
27	P0.25	I/O	Configurable I/O
28	P0.30	I/O	Configurable I/O
29	P0.31	I/O	Configurable I/O
30	P0.17	I/O	Configurable I/O
31	P0.19	I/O	Configurable I/O
32	GND	GND	Ground
33	NC	NC	NC
34	GND	GND	Ground
35	P0.20	I/O	Configurable I/O
36	P0.18	I/O	Configurable I/O

37	P0.14	I/O	Configurable I/O
38	P0.13	I/O	Configurable I/O
39	P0.10	I/O	Configurable I/O
40	GND SLUG	GND	Ground PAD

<Table 5 : PIN descriptions>

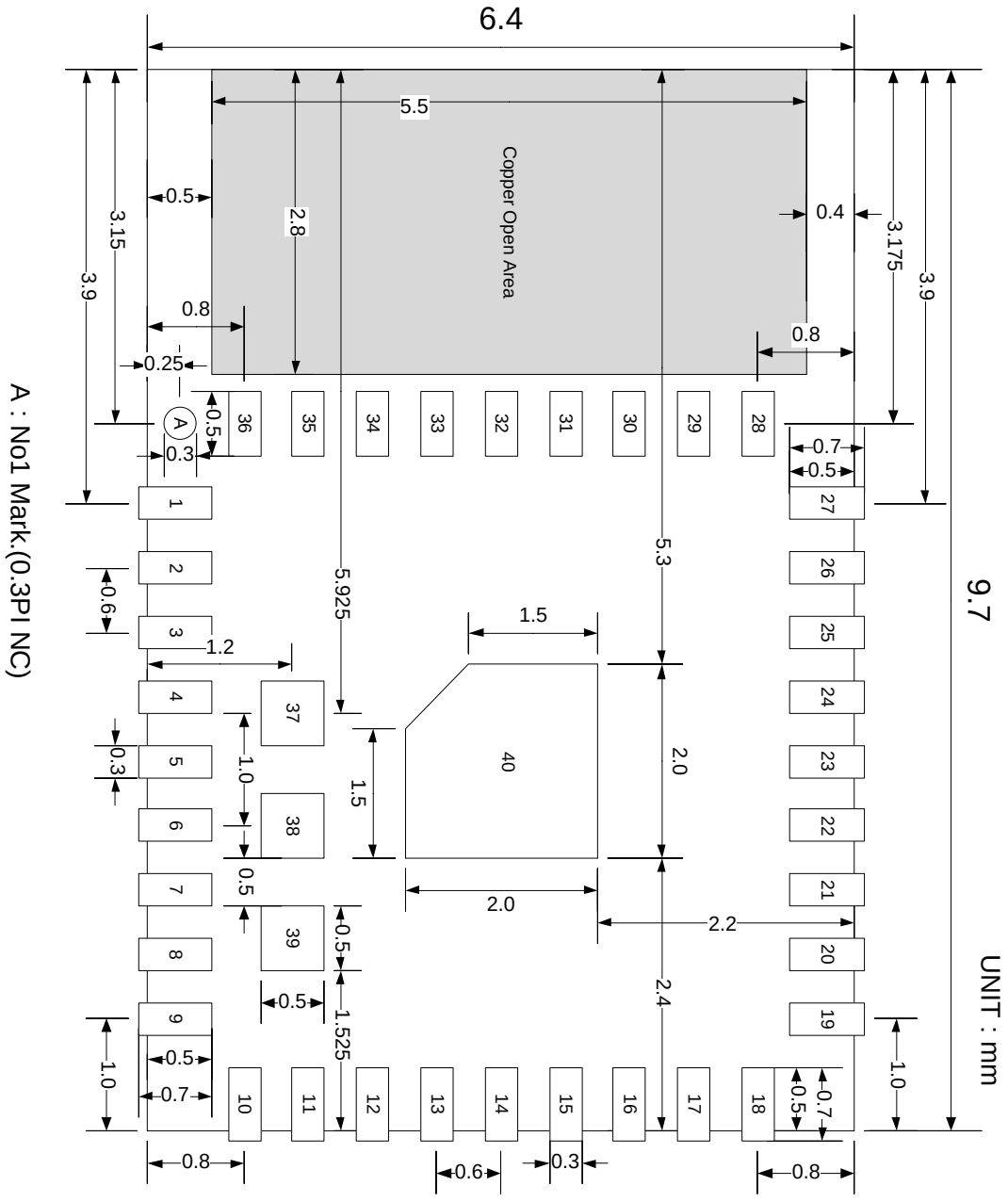
4. Physical Dimensions



- Top View (Bottom pad)

<Figure 4. Physical dimension>

5. Layout

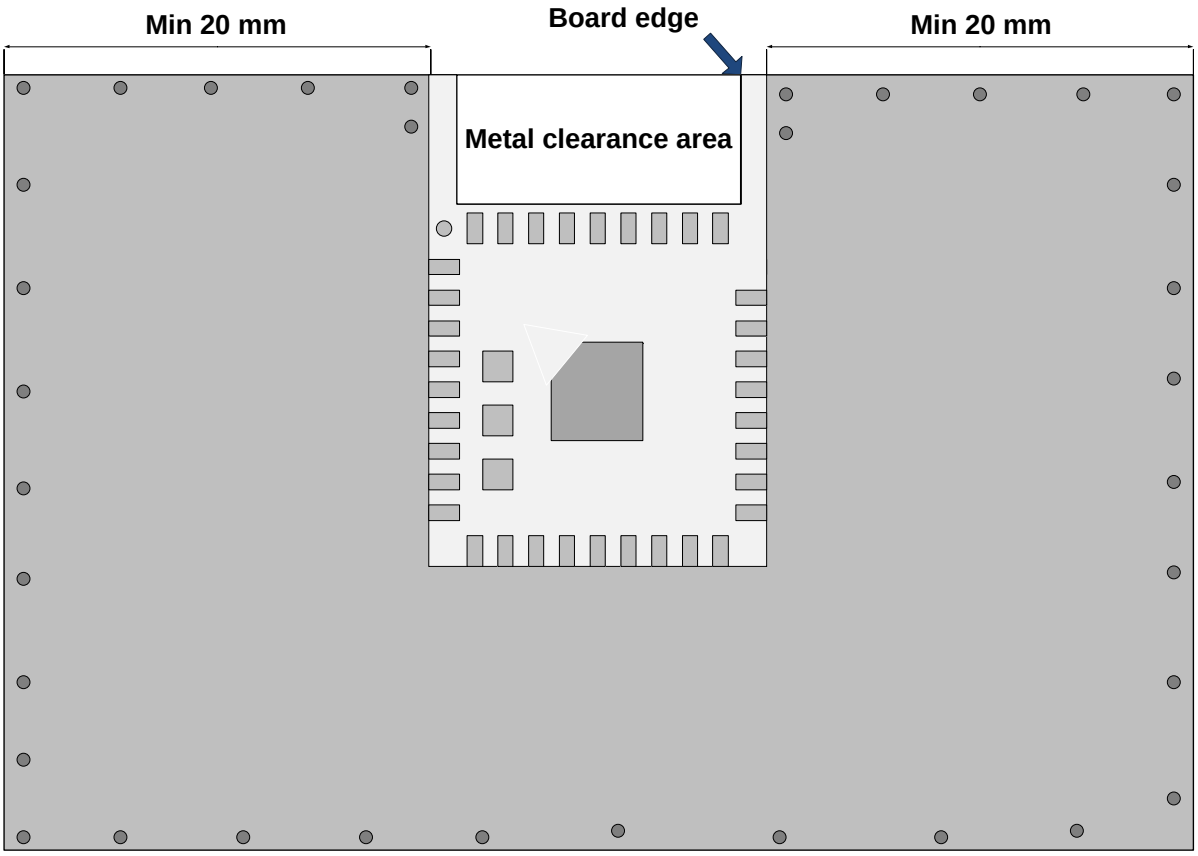


- Top View (Bottom pad)

<Figure 5. Layout>

5.1 Layout Guide

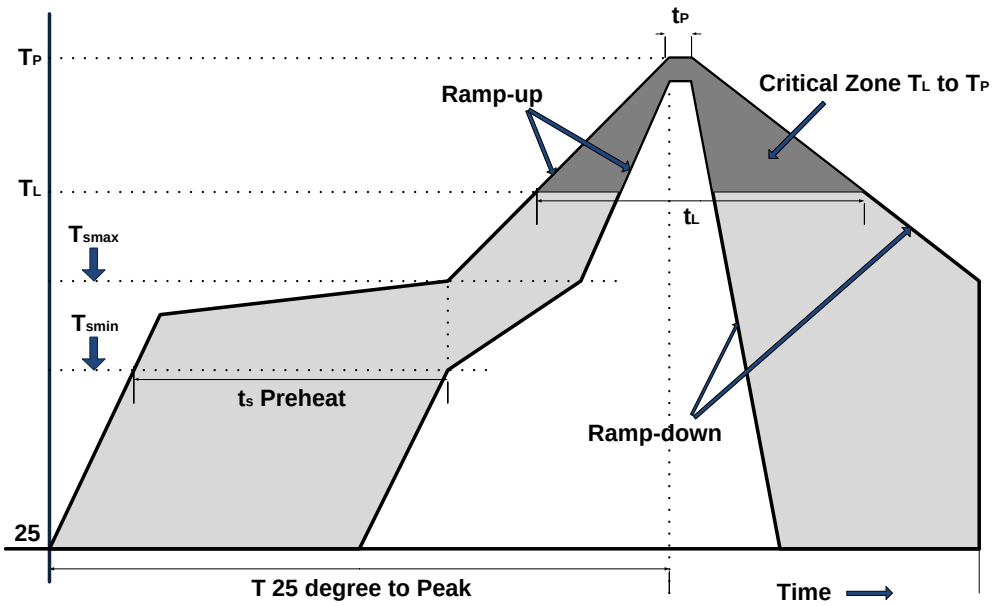
To achieve best radio performance for UTO-NBL-51MA, it is recommended to use the module at the edge of the PCB as shown in Figure 6. Do not place any metal (traces, components, etc.) within the clearance area of the antenna. Connect all the GND pins directly to a solid GND plane. Place the GND vias as close to the GND pins as possible. Do not place plastic or any other dielectric material in touch with the antenna.



<Figure 6. Recommended layout>

6. Re-flow Temperature time profile

The data here is given only for guidance on solder and has to be adapted to your process and other re-flow parameters for example the used solder paste. The paste manufacturer provides a re-flow profile recommendation for his product.



<Figure 7. Soldering Temperature time profile>

Preheat		Main Heat		Peak	
Tsmax		TLmax		tpmax	
Temperature	Time	Temperature	Time	Temperature	Time
Degree	sec	Degree	sec	Degree	sec
150	100	217	90	260	10
		230	50		
Parameter				Value	Unit
Average ramp-up rate				3	Degree/sec
Average ramp-down rate				6	Degree/sec
Max. Time 25 degree to Peak Temperature				8	Min.

<Table 6 : Soldering temperature parameters>

Opposite side re-flow is prohibited due to module weight. Devices will withstand the specified profile and will withstand up to 1 re-flows to a maximum temperature of 260 degree. The re-flow soldering profile may only be applied if the UTO-NBL-51MA resides on the PCB side looking up. Heat above the solder eutectic point while the UTO-NBL-51MA is mounted facing down may damage the module permanently.

UTOVERTEK Co., Ltd. RM 210, KETI Business Incubator, 25 seanari-ro, Bundang-gu, Seongnam-si, Gyeonggi-do 463-816 Korea.

Phone : +82 31 781 2593

Fax : +82 31 781 2594

E-mail : sales@utovertek.com

www.utovertek.com